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# BACKGROUNDER

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## BUMPLESS BUILD-UP LAYER PACKAGING TECHNOLOGY

BBUL ("Bumpless Build-Up Layer") packaging is a new microprocessor packaging technology that has been developed by Intel. It is called *bumpless* because, unlike today's packages, it does not use tiny solder bumps to attach the silicon die to the package wires. It has *build-up layers* because the package is 'grown' (built up) around the silicon die, rather than being manufactured separately and bonded to it. Both of these concepts will be detailed in this backgrounder.

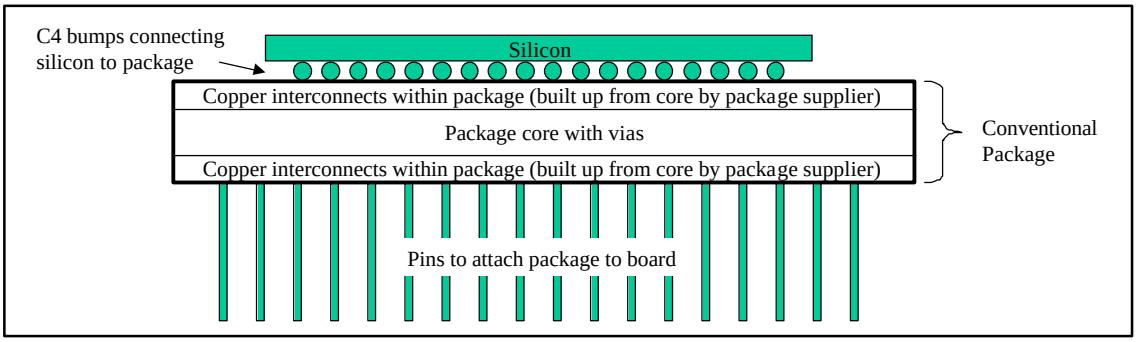
BBUL packaging offers a number of advantages over today's packaging technologies. It is thinner and lighter. It offers certain electrical performance and power advantages. And, with BBUL, it is possible to tightly interconnect multiple chips (processors, memories, etc.) inside the same small package.

Packaging advances are a key element of Intel's strategy to reach the billion transistor 20 GHz microprocessor in the second half of this decade. Packaging is as important as other advances that Intel is making, such as in transistor architecture, interconnects, dielectrics and lithography. As with other advanced technology announcements, from Intel years of work lie ahead before this technology may become suitable for volume manufacturing.

## Today's Microprocessor Packaging

A silicon chip is useless without its package. The package delivers the power the chip needs and transfers all the information into and out of the chip to the motherboard. It draws heat away from the silicon transistors to keep them running at their peak performance and it protects the silicon chip from damage from the environment.

As can be seen in the diagram below, today's package is connected to the silicon die with a set of C4 solder bumps. When the silicon is manufactured, these C4 bumps are the last structures that are put on. It is these bumps that are used later to connect the silicon to the package..

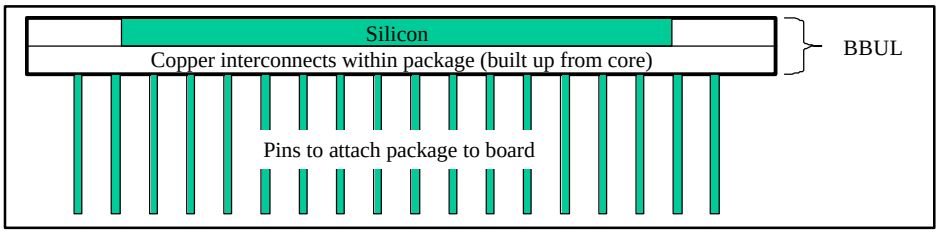



The package makes electrical connection between the bumps and the pins, which are spaced much farther apart than the C4 bumps. The package consists of 3 layers. The middle layer, known as the core, is a sheet of plastic with vias (copper interconnects that pass vertically through the core). The top and bottom layers of the package contain a network of copper interconnects that make sure the right C4 bump is routed to the right pin.Manufacturing of the package starts with the core. Vias are placed in the core by laser-drilling holes and filling them with copper. Then the interconnect layers are built up on both sides of the core. The specifications of the vias and interconnect layers are unique to each chip.

Once the pins are attached, the package is ready for insertion into the board. In a variation called BGA (ball grid array) the pins are replaced by balls which attach to the surface of the board.

## BBUL Packaging Technology

In BBUL packaging, the top interconnect layer in the package is not needed and neither are the C4 bumps. Instead, the silicon is embedded in the package core and only the lower interconnect layer needs to be built up. Hence the term *Bumpless Build-Up Layer*.




## BBUL Packaging Advantages

BBUL packaging offers a number of advantages over the conventional package:

- *Thinner and lighter*. A BBUL package is thinner because the silicon is embedded in the package core rather than sticking out on its surface. A thinner package is clearly lighter. These attributes are obviously important in small form factors.

- *Higher performance and/or lower power*. Because interconnects are shorter, they have reduced inductance. Also, capacitors, which are placed on the pin side of the package (not shown in diagrams), are closer to the silicon. This facilitates better power delivery. Together, these allow the silicon to run at a higher frequency, hence improving its performance. They can also allow the chip to operate at a lower voltage due to the reduced electrical noise. As power dissipation reduces quadratically with the voltage, the potential power savings could be significant, which is very important in mobile applications.

- *Higher interconnect density*, allowing more interconnects to/from the silicon. As processors become more complex, they will require more interconnects. C4 bumps were reaching the limit; BBUL package limits are far higher.

- *Better capability to route signals from one part of the die to another*. While intra-die signal routing is done in conventional packages as well, the lack of C4 bumps in a BBUL package allows for a closer, better connection. This can increase transistor density on the silicon, and hence performance of the chip.

- *Allows multiple chips in same package.* Multiple silicon die can be embedded in the same BBUL package. The interconnect layer can make connections from the die to the pins, and also among the die. One possibility, for example, is to embed both a CPU and chip set into the same package.

**Evaluating A New Technology**

BBUL is a great technology and Intel is in the early stages of exploring the supply-chain and infrastructure challenges of bringing it to market.

As with any new technology, there are numerous technical issues that need to be resolved before volume production can begin. This process must be refined and perfected so that yields reach an acceptable level. There are questions of reliability which Intel is investigating. Finally, Intel and its customers need to qualify any new process and product.